Data Book
ZF SystemCard 5MX

Embedded System Card
based on the
5MX Z-chipset

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General Description

The ZF SystemCard 5MX is a full-featured embedded system computer utilizing the low power, high performance 5MX Z-chipset. It is a Pentium® Class PCI/ISA-compatible motherboard including standard peripheral interfaces. Its small size, low power consumption, and rugged construction makes it ideal for embedded systems. You can develop software directly on a SystemCard 5MX or on a desktop PC and transfer your code directly to the embedded system with little or no modification.

The SystemCard 5MX includes all standard motherboard functions, serial and parallel I/O, floppy and EIDE disk controllers, a high-performance CRT/flat-panel video controller, a 100Base or 10BaseT Ethernet interface, an internal resident Flash disk for program storage, SoundBlaster compatible audio, PC/104 and PCI expansion buses, a standard and extended BIOS, 5-wire touchscreen (optional), and USB ports.

For many systems, the ROM-BIOS and resident Flash disk eliminate the need for rotating media (such as a floppy or hard disk) for application program storage.

Industry Standard Compatibility

The SystemCard 5MX expansion bus conforms to the popular PC/104 standard. It allows you to easily integrate a wide variety of low-cost PC/104 peripherals in your embedded system. The SystemCard 5MX has a non-stackthrough PC104 connector.

The SystemCard 5MX also supports the PCI expansion bus and has two USB ports.

The board's PC-compatible serial ports, parallel port, floppy interface, and hard disk interface allow you to use standard hardware, cables, and software libraries in your development program.

Features

64-bit 180 MHz CPU

- Full 64-bit internal architecture, cost-effective 16-bit external ISA bus and a 32-bit external PCI expansion bus
- Virtual memory, paging, and hardware-enforced protection.
- Integrated Floating Point Unit (FPU)

PC Core Logic

- AT-compatible DMA controllers, interrupt controllers, timer/counters .
- AT keyboard controller.
- 16KB write-back L1 cache
- PS2 mouse port
- Y2K Compliant Real-time clock.

DRAM Controller

- High performance 64-bit synchronous DRAM controller.
- Up to 160MB - 128MB in DIMM socket and 32MB soldered on board (only on the netDisplay version).
- Shadowed BIOS for optimum performance.

Serial Ports

- Four 16650 (16550-compatible) RS232C serial ports (One can be either RS232 or RS485)
- Two 16550-type RS232C serial ports

Parallel Port

- One fully-compatible PC/AT parallel port
- Supports bi-directional operation
- ECP/EPP modes available

Floppy Disk Controller

- Software compatible with 765B floppy controller and PC BIOS.
- Supports all high density PC floppy formats.
- Only supports one floppy drive
- FFC connector provided for drive connection.

EIDE Hard Drive Interface

- Standard 40-pin interface to EIDE hard disk drive.
- Supports up to three EIDE drives: hard drive, CD-ROM, and Compact Flash Disk.

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CRT/Flat-Panel Controller

- 2 Mbytes of system DRAM is used for Video
- Full VGA and VESA mode support
- 64-bit Windows accelerator
- 64-bit Graphic processing
- CRT output monitors with resolutions up to 1280 x 1024
- Supports dual scan color STN flat panels up to 1024 x 768 with optional daughter card
- Direct interface to color TFT panels
- Supports 18-bit data interfaces
- Supports power-sequencing controls for Vdd, Vee, and +12V to inverter for backlights

Ethernet Controller

- Based on the Realtek RTL8139A PCI Fast Ethernet controller with Power Management
- 100BaseT (twisted-pair), 10/100Mb/s
- Full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control
- Compliant to PCI Revision 2.1
- Supports ACPI, PCI power management
- Driver support includes Novell NetWare, Microsoft Windows 95, Windows 98, Microsoft LAN Manager, SCO UnixWare, IBM LAN Server, SunSoft PC-NFS, SunSoft Solaris, Artisoft LANtastic, Banyan Vines

Universal Serial Bus (USB)

- Two independent USB interfaces
- Open Host Controller Interface (OpenHCI) specification compliant

Audio Support

- SoundBlaster compatible
- 16-bit stereo FM synthesis
- OPL3 emulation
- Microphone input
- Headphone output (up to 300mW audio power)
- CD ROM sound input

Touchscreen Controller (netDisplay version only)

- Based on ELO E271-Coach Touchscreen controller
- 5-wire touchscreen
- Driver support for DOS, Win3.1, Win95, Win98, WinNT, LINUX, and OS2.

Solid-State Flash Storage

- On board 1.4M byte Flash EPROM, available for OS and OEM software

Compact Flash Socket

- Currently 2M to 96M bytes storage. Size limit will change with future technology.
- Can be configured to be the boot drive

Configurable Memory Sockets

- One 32-pin byte-wide memory socket
- Supports DiskOnChip.
- Supports popular 5V JEDEC Flash EPROMs and Non-volatile NVRAM devices
- BIOS configurable addressing

PC BIOS

- Standard and extended PC BIOS functionality.
- Easy to upgrade using ZF Embedded's unique utilities.

Embedded Disk Operating System

- Supports most PC/AT-compatible operating systems, including MS-DOS
- Support for standard desktop software, including Windows 3.1, Windows 95, Windows 98

Expansion Buses

- Supports the PC/104 expansion bus (non stack through version)
- Add up to three PC/104 modules
- Supports PCI 2.1 compliant expansion bus
- Supports PCI initiator-to-ISA and ISA master-to-PCI cycle translations

Power Monitor

- Brownout protection, provides reliable reset signal if 3.3 volt power fluctuates.

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Electrical Specifications

- Requires +5VDC @ 2.2amps (32MB DRAM)

Mechanical Specifications

- 5.75” x 8.00” (146mm x 203mm)
- PC/104 bus compliant with PC/104 V2 specification.
- Standard ribbon cable connectors for EIDE, serial, and parallel interfaces. Floppy uses a FFC connector.
- Standard connectors for P/S2 keyboard, CRT, 100Base-T Ethernet, USB, Microphone, and Headphones

Environmental Specifications

- Processor case operating temperature: 32F to 158F (0C to 70C).
- Storage temperature: -67F to 185F (-55C to 85C).
- Weight: 10 oz (284 gm).

ORDERING INFORMATION

SCX-5MX-Q-01 — ZF SystemCard 5MX. SystemCard form factor, includes 5MX Z-chipset, 2MB built-in Flash, SVGA controller, 10/100Base T Ethernet controller, SoundBlaster compatible, Compact Flash interface, speaker, BIOS and Embedded DOS-ROM.

SCX-5MX-K-01 — ZF SystemCard 5MX Development Kit. SystemCard form factor, includes 5MX Z-chipset, 32MB DRAM SIMM, 2MB built-in Flash, SVGA controller, 10/100BaseT Ethernet controller, SoundBlaster Compatible, Compact Flash interface, speaker, BIOS, technical manuals, cables, and utility software.

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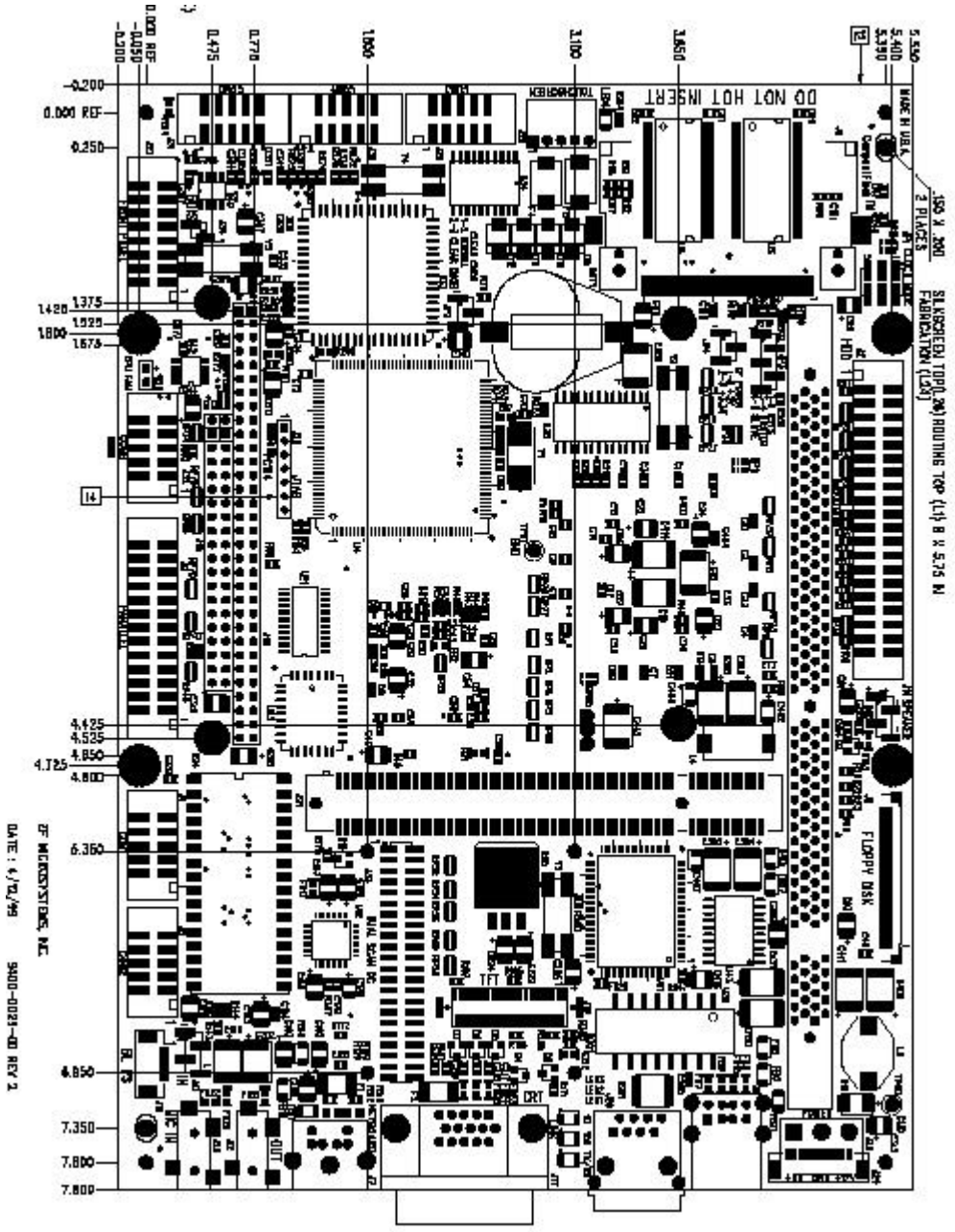


Figure 1. Board Dimensions

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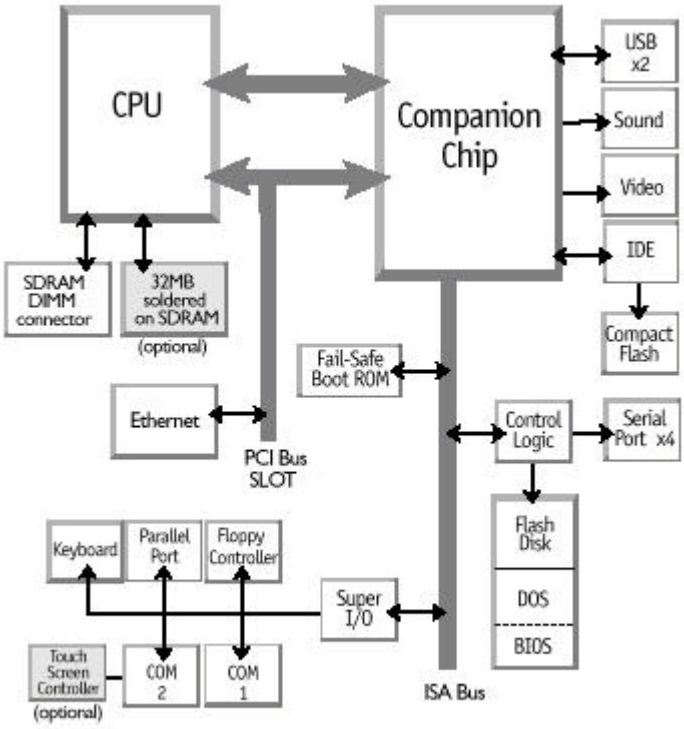


Figure 2. System Block Diagram

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Connector Summary

Table 1 summarizes the SystemCard 5MX connectors, J1 through J35.

Connector	Function	Type	Refer to
J1	Memory Expansion	168-pos DIMM socket	Page 8DRAM Interface
J2	EIDE	40-pos Dual Row, .100” centers	Page 16
J3	CompactFlash Socket	50-pos, SanDisk Standard	Page 16
J4	Serial 1	10-pos Dual Row, .100” centers	Page 11
J5	Serial 2	10-pos Dual Row, .100” centers	Page 11
J6	USB Ports 1 & 2	Stacked USB	Page 26
J7	Keyboard	6-pos, Miniature DIN	Page 10
J8	Floppy	26-pos ZIF FFC	Page 15
J9	Parallel 1	26-pos Dual Row, .100” centers	Page 12
J10	CD In or Line In	4-pos Single Row, .100” centers	Page 26
J12	Headphone Out	Phone jack	Page 26
J14	Speaker	4-pos Single Row, .100” centers	Page 25
J15	Flat Panel	41-pos 2mm centers	Page 21
J16	Flat Panel Backlight Power	5-pos Single Row, 1.25 mm centers	Page 21
J17	VGA	15-pos D-sub	Page 20
J18	PC/104 A/B	64-pos Dual Row, .100” centers(non stackthrough)	Page 27
J19	PC/104 C/D	40-pos Dual Row, .100” centers(non stackthrough)	Page 27
J20	JTAG	6-pos Single Row, .100” centers	Factory use only
J21	PCI Expansion Bus	120-pos PCI connector	Page 32
J23	Power	3-pos Screw Terminal, 5mm	Page 9
J24	Alternate Power	10-pos, 1.25mm centers	Page 9
J26	Ethernet	RJ45	Page 24
J28	Touchscreen	5-pos Single Row, .100” centers	Page 24
J29	Serial 3	10-pos Dual Row, .100” centers	Page 11
J30	Serial 4	10-pos Dual Row, .100” centers	Page 11
J31	Serial 5	10-pos Dual Row, .100” centers	Page 11
J32	Serial 6	10-pos Dual Row, .100” centers	Page 11
J33	Dual Scan Interface	44-pos Dual Row,	Page 21
J35	Microphone In	Phone jack	Page 26

Table 1. Connector Summary

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Jumper Summary

The SystemCard provides a number of jumper options to configure features on the board. The jumpers, labeled "JP*n*", are configured with 2mm shorting blocks. Table 1 shows a summary of the jumpers, their functions, and the factory default settings. For jumper options with more than two pins, default shorted pin-pairs are listed as *n1-n2*.

Jumper	Function	Default
JP1	Clock mode – this jumper is used to set the core clock speed. Speed / Pins 1-2 / Pins 3-4 / Pins 5-6 120MHz / On / On / On 133MHz / Off / On / On 180MHz / On / On / Off Reserved / Off / On / Off	1-2 On 3-4 On 5-6 Off
JP2	Clear CMOS 1-2 Normal operation 2-3 Clear CMOS	1-2
JP3	CompactFlash 1-2 M-Systems CompactFlash Disk present 3-4 Master 4-5 Slave	3-4
JP4	CompactFlash Voltage 1-2 5V 2-3 3.3V	1-2
J34	Fail Safe ROM BIOS	Off

Table 2. Jumper Summary

DRAM Interface

The SystemCard 5MX is supplied with 32M bytes of DRAM soldered on board (netDisplay version only). A 168 pin DIMM socket can be populated to expand the memory to 160M bytes.

SETTING MEMORY SIZE

The BIOS automatically senses the amount of memory installed in your system and displays that information on the Setup configuration page. There is no user setting.

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Power and Utility Connectors

+5 Volt and +12 Volt power are supplied through the 3-pin screw terminal connector, JC1. The SystemCard 5MX also has an alternate 10 pin power connector, J24, which also supplies –5 and –12 volts. Contact your ZF Embedded sales representative for details.

+5 Volts is used for the board's main logic supply. +12V is used to provide power for the CPU fan and a flat panel (if connected).

Table 3 lists the power pins on JC1. Table 4 lists the power pins on J24.

Pin	Description
1	+12 Volts
2	Ground
3	+5 Volts

Table 3. Power Connector, JC1

Pin	Description
1	+5 Volts
2	+5 Volts
3	+5 Volts
4	Ground
5	Ground
6	Ground
7	+5 Volts SB
8	-12 Volts
9	-5 Volts
10	+12 Volts

Table 4. Alternate Power Connector, J24

The J24 connector is from Molex, part number 53261-1090 and a typical mating connector is Molex, part number 51021-1000.

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KEYBOARD

The SystemCard 5MXprovides the standard keyboard signals on 6 pin miniature DIN connector, J7. Table 5 shows signal names, functions, and pin connections to J7.

J7	Signal Name	Function
1	KBDATA	Keyboard Data
2	N/C	N/C
3	KBGND	Ground return
4	KBPWR	+5 Volts
5	KBCLKX	Keyboard Clock
6	N/C	N/C

Table 5. Keyboard Connector, J7

REAL-TIME CLOCK BATTERY

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time, date, and CMOS memory values when power is off. A 195 mAh lithium cell is supplied with the board, providing up to 7 years of power for the real-time clock and CMOS memory.

If the battery fails and +5 Volt power is removed, the RTC will lose the current time/date and the Setup data will be lost.

Serial Ports

The SystemCard 5MX has six serial ports on board. There are five full-featured PC-compatible asynchronous RS232C serial ports and one RS232/RS485 serial port. The serial ports are treated as COM1, COM2, COM3, and COM4 devices by DOS. COM5 and COM6 are not recognized by DOS, only Windows. COM5 & COM6 can be used by DOS if they are accessed directly by customer software.

Standard system resources are allocated to the serial ports, as shown in Table 6:

Note: COM2 is not available if the touchscreen interface is installed.

Serial Port	Connector	Typical Usage	I/O Address	Standard Interrupt	Boot Defaults
Serial 1	J4	COM1	3F8h–3FFh	IRQ4 (shared)	IRQ4
Serial 2	J5	COM2	2F8h–2FFh	IRQ3 (shared)	IRQ3
Serial 3	J29	COM3	3E8h–3EFh	Programmable	IRQ7
Serial 4	J30	COM4	2E8h–2EFh	Programmable	IRQ9
Serial 5	J31	COM5	4220h–4227h	Programmable	IRQ3
Serial 6	J32	COM6	4228h–422Fh	Programmable	IRQ3

Table 6. Serial Port Resources

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RS232 SERIAL PORT CONNECTORS

The RS232 serial ports (Serial 1, Serial 2, Serial 3, Serial 4, Serial 5, and Serial 6) are brought out to 10-pin dual-row ribbon-cable connectors J4, J5, J29, J30, J31, and J32. The connector pins are arranged to make it easy to construct a simple straight-through ribbon cable to a panel-mount DB-9 connector.

A full complement of input and output handshaking lines is implemented. Signals are at standard RS232C levels. Power for the RS232 voltage levels (-9V > x > +9V) is converted on-board from the +5V supply.

Pinouts for the serial connectors and for standard DB-9 connectors are shown in Table 7.

J4, J5, J29, J30 J31, J32	DB-9 Pin	Signal	Function	In/Out
1	1	DCD	Data Carrier Detect	Input
3	2	RXD	Receive Data	Input
5	3	TXD	Transmit Data	Output
7	4	DTR	Data Terminal Ready	Output
9	5	GND	Signal Ground	
2	6	DSR	Data Set Ready	Input
4	7	RTS	Request To Send	Output
6	8	CTS	Clear To Send	Input
8	9	RI	Ring Indicator	Input
10		N/C	Ground	

Table 7. Serial Port Connectors, J4, J5, J29, J30, J31, J32

Serial 1 and 2 are always enabled and require no set up. Serial 3 through Serial 6 are enabled at power up.

RS485 SERIAL PORT CONNECTOR, J32

Serial 6 can be configured as either an RS 232 or a RS485 serial port based on a 16550-equivalent UART. You can use the RS485 port, configurable to RS485 half or full duplex, as a low cost, easy-to-use communications and networking multi-drop interface. It can be used in a wide variety of embedded applications requiring low-to-medium-speed data transfer between two or more systems.

The following are some examples of interconnection schemes that can be used to take advantage of the RS485 port:

- **One-way Broadcast** — A single device, set in transmit mode, uses an RS485 signal pair to transmit data to many receiving devices.
- **Simple Bi-Directional Communication (half or full duplex)** — Two devices use a single RS485 bi-directional pair for half-duplex or two pairs for full-duplex, two-way transmission of data. In half-duplex mode, only one device is permitted to talk at any one time. A port is placed in transmit mode under control of the network software, either by a simple alternation scheme or by messages contained within data packets.
- **Multi-Drop Network** — More than two devices share an RS485 signal pair, for both transmission and reception of data. Only one device is permitted to talk at any one time. All RS485 transceivers are placed in receive mode except the one permitted to transmit. One popular protocol for managing who is the transmitter is by a “token” passing scheme. Each node is assigned an ID number. Whichever node transmits also sends the ID of the next node allowed to transmit. If a node does not need to transmit, it

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immediately sends the “token” indicating who can talk next. Time-outs can be implemented in software to prevent a lockup should a node fail to pass the token properly.

The RS485 serial port is brought out to a 10-pin dual row connector. Table 8 lists the pinout of this connector.

Signal Name	Pin	Description
B	4	Signal B (-); Bidir in Half Duplex, Out in Full Duplex
A	5	Signal A (+);Bidir in Half Duplex, Out in Full Duplex
B	6	Signal B (-); Input in Full Duplex
A	7	Signal A (+); Input in Full Duplex
Ground	9	Ground

Table 8. RS485 Connector, J32

Serial port 6 is configured as a RS232 port. Contact the factory it you wish to reconfigure this port as RS485.

SERIAL PORT INTERRUPT SHARING

The COM1 and COM2 serial port interrupt request lines comply with the interrupt sharing scheme described in the PC/104 Version 2.3 specification. For a copy of the PC/104 Version 2.3 specification, visit the PC/104 Consortium web site (www.controlled.com/pc104).

The interrupt request lines from Serial 1 and Serial 2 are buffered with open collector buffers and internally connected to inputs IRQ4 and IRQ3 respectively. Internal 1000 ohm termination resistors hold the interrupt signals at logic 0 until an interrupt occurs. Other interrupt sources can be wire-ORed with either of these IRQ lines as long as they also follow the PC/104 interrupt sharing convention. The interrupt request signals appear on the PC/104 bus.

Note: The 1000 ohm pull-down resistor for each interrupt is provided on the board. Do not attach an external pull-down resistor.

Parallel Port

The SystemCard 5MX parallel port is fully compatible with the PC/AT parallel port. In the extended mode, it functions as PS/2-like bi-directional ports.

The parallel port uses the following PC resources (Table 9):

Parallel Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	J9	LPT1	378h – 37Fh	IRQ7

Table 9. Parallel Port Resources

PARALLEL PORT SIGNALS

The parallel port output signals provide up to 14 mA drive current (active low). 180 pF capacitors are connected from each data line to ground for noise suppression.

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The parallel port signals appear on J9, 26-pin dual-row ribbon-cable connector. The ports may be cabled to appear on standard PC DB-25 connectors.

Table 10 shows the parallel port signals that appear on J9 and the equivalent pinout on the DB-25S connector.

J9	DB-25S Pin	Signal	Function	In/Out
1	1	PPSTBX	Output Data Strobe	Output
2	14	PPAFDX	Auto Feed	Output
3	2	PPD0	Data Bit 0	I/O
4	15	PPERRX	Printer Error	Input
5	3	PPD1	Data Bit 1	I/O
6	16	PPINITX	Initialize Printer	Output
7	4	PPD2	Data Bit 2	I/O
8	17	PPSLINX	Selects Printer	Output
9	5	PPD3	Data Bit 3	I/O
10	18	GND	Signal Ground	N/A
11	6	PPD4	Data Bit 4	I/O
12	19	GND	Signal Ground	N/A
13	7	PPD5	Data Bit 5	I/O
14	20	GND	Signal Ground	N/A
15	8	PPD6	Data Bit 6	I/O
16	21	GND	Signal Ground	N/A
17	9	PPD7	Data Bit 7	I/O
18	22	GND	Signal Ground	N/A
19	10	PPACKX	Character Acknowledged	Input
20	23	GND	Signal Ground	N/A
21	11	PPBUSY	Printer Busy	Input
22	24	GND	Signal Ground	N/A
23	12	PPPE	Out Of Paper	Input
24	25	GND	Signal Ground	N/A
25	13	PPSLCT	Printer Selected	Input
26	N/A	CHGND	Chassis Ground	N/A

Table 10. Parallel Port Connectors, J9

PARALLEL PORT REGISTERS

Table 11 summarizes the parallel port register interface. In this table, “base” indicates the port’s base address, for example, 378h.

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Port Function	Address
Data Port	Base Address + 00h
Status Port	Base Address + 01h
Control Port	Base Address + 02h
EPP Address Port	Base Address + 03h
EPP Data Port 0	Base Address + 04h
EPP Data Port 1	Base Address + 05h
EPP Data Port 2	Base Address + 06h
EPP Data Port 3	Base Address + 07h

Table 11. Parallel Port Register Address Map

Port	D0	D1	D2	D3	D4	D5	D6	D7	Note
Data	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
Status	TMOUT (Note 1)	0	0	ERR-	SLCT	PE	ACK-	BUSY-	1
Control	STROBE	AUTOFD	INIT-	SLIN	IRQE	PCD	0	0	1
EPP Addr	AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	2
EPP Data 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Table 12. Parallel Port Register Bit Definitions

Note 1: These registers are available in all modes.

Note 2: These registers are only available in EPP mode.

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Note 3: Bit definitions:

PDn	Parallel port data
TMOUT	10 µS time-out has occurred on the EPP bus. (This bit is only valid in EPP mode.)
ERR-	0 means and error has been detected.
SLCT	1 means that the printer is online.
PE	1 means that there is no paper in the printer.
ACK-	0 means that the printer has accepted a character and can now receive another.
BUSY-	0 means that the printer is busy. It is the complement of the level on the BUSY input.
STROBE	1 means there is valid data on the PDn bus. This bit is inverted and output onto the STROBE- pin.
AUTOFD	1 causes the printer to generate a linefeed after each line. This bit is inverted and output onto the AUTOFD- pin.
INIT-	0 causes printer to initialize.
SLIN	1 selects the printer. This bit is inverted and output onto the SLCT- pin.
IRQE	1 enables interrupts. An interrupt is generated on the positive-going ACK- input.
PCD	In bi-directional mode, 0 means output, 1 means input. Only valid in extended mode.

Table 13. Parallel Port Bit Definitions

Floppy Interface

An AT-compatible floppy drive interface is supplied on J8. This interface allows cable connection to one floppy drive. In AT-compatible systems, the BIOS and DOS support this drive as A: or B:. This is configured using the BIOS Setup function.

Table 14 shows the PC resources used by the floppy subsystem.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2–DACK2	DMA Controller Channel

Table 14. Floppy Interface Resources

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The floppy drive interface supports the standard 1.44M floppy disk format. You must specify the type of drive connected to the floppy interface in the BIOS CMOS Setup. Press <Del> during the Power-On Self Test (POST) to enter Setup. The first drive typically appears to DOS as drive A:, and the second drive as B:.

Floppy drives are connected to a system using ribbon cables. The SystemCard 5MX floppy interface only supports one floppy drive. The board's internal Resident Flash Disk (RFD), if enabled, is configured as a floppy drive. You can decide to make the floppy drive as Drive A: and the RFD as Drive B: or visa versa.

Table 15 lists the signals on the J8 floppy interface.

Pin	Signal Name	Function	In/Out
2	INDX	Index Pulse	In
4	DRX0	Drive Select 1	Out
6	DSKCHG	Disk Change	In
10	MTRX0	Motor On 0	Out
12	DIRX	Direction Select	Out
14	STEPX	Step Pulse	Out
16	WDATAX	Write Data	Out
18	WGATE-	Write Gate	Out
20	TRKX0	Track 0	Input
22	WPX	Write Protect	Out
24	RDATA-	Read Data	Input
26	HDSEL-	Head Select	Out
1, 3, 5	Vcc	Power	N/A
7-9, 11,13	N/C	Not Connected	N/A
15– 25 (Odd)	Ground	Ground	N/A

Table 15. Floppy Drive Connector, J8

EIDE Interface

The SystemCard 5MX is supplied with two EIDE Interfaces at connectors J2 and J3. The primary EIDE interface, J2, is the standard interface used in PC-compatible systems for hard disk drives, CD-ROM drives, and certain other peripherals. The secondary EIDE interface, J3, is dedicated to a CompactFlash device.

Up to two drives can be connected in a master-slave arrangement to J2. Generally, the first hard disk drive (master drive) will appear as the C drive to DOS. The second drive (slave drive), if attached, will appear as drive D. J3 will only support one CompactFlash disk.

If you use the SanDisk CompactFlash, it is installed as an IDE drive in the system. Jumper this device as a master device.

Table 16 lists the resources used by the EIDE interface.

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Resource	Function
I/O Address 1F0h-1F7h, 3F6h	Primary IDE Registers
170h – 177h, 376h	Secondary IDE Registers
IRQ14	Primary IDE Interrupt
IRQ15	Secondary IDE Interrupt

Table 16. EIDE Interface Resources

Use Setup to enable your attached hard drives. You must match the drive parameters in Setup with the actual parameters of your connected drive(s).

EIDE drives are typically attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard 0.1 inch-spacing connector and the smaller connector on the drive. These generally are supplied with the drive.

The pinout for the primary EIDE interface, J2, is shown in Table 17.

Note: Due to drive manufacturer's different implementations of the master/slave arrangement, it may not be possible to properly configure two IDE drives from different sources to share the EIDE bus.

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Pin	Signal Name	Function	In Out	Pin	Signal Name	Function	In Out
1	IDEPRSTX	Reset signal from host	Out	21	IDEPDREQR	DMA Request 0	In
2	GND	Ground		22	GND	Ground	
3	IDEPDR7	Data bit 7	I/O	23	IDEPIOWX	Write strobe	Out
4	IDEPDR8	Data bit 8	I/O	24	GND	Ground	
5	IDEPDR6	Data bit 6	I/O	25	IDEPIORX	Read strobe	Out
6	IDEPDR9	Data bit 9	I/O	26	GND	Ground	
7	IDEPDR5	Data bit 5	I/O	27	IDEPIORDYR	IO Channel Ready	In
8	IDEPDR10	Data bit 10	I/O	28	ALE	Address Latch Enable	GND
9	IDEPDR4	Data bit 4	I/O	29	IDEPDACKX	DMA Acknowledge 0	Out
10	IDEPDR11	Data bit 11	I/O	30	GND	Ground	
11	IDEPDR3	Data bit 3	I/O	31	IDEPINTR	Drive interrupt request	In
12	IDEPDR12	Data bit 12	I/O	32	IDEPIOCS16X	I/O Chip Select 16	In
13	IDEPDR2	Data bit 2	I/O	33	IDEPA1	IDE Address 1	Out
14	IDEPDR13	Data bit 13	I/O	34	RSVD	Reserved	N/C
15	IDEPDR1	Data bit 1	I/O	35	IDEPA0	IDE Address 1	Out
16	IDEPDR14	Data bit 14	I/O	36	IDEA2	IDE Address 2	Out
17	IDEPDR0	Data bit 0	I/O	37	IDEPCS0X	IDE Chip Select 0	Out
18	IDEPDR15	Data bit 15	I/O	38	IDEPCS1X	IDE Chip Select 1	Out
19	GND	Ground		39	HDDLED0		
20	KEY	Keyed pin	N/C	40	GND	Ground	

Table 17. Primary EIDE Drive Connector, J2

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A connector is provided for a CompactFlash (CF) card on the secondary EIDE interface. Connected to the IDE bus, the CF cards can provide 60M bytes or more of removable solid-state disk storage.

If you use the CF drive, it takes the place of an IDE hard disk drive in your system. Use Setup to configure your system for the IDE drives you use.

The CF drive can be an IDE master. To boot from the CF drive, it must be formatted as a bootable drive and configured as master.

In the Setup Screen, this device should be configured as the secondary master (IDE2). IDE2 should be configured as type 2, physical

The pinout for the Compact Flash, J3, is shown in Table 18

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Pin	Signal Name	Function	In Out	Pin	Signal Name	Function	In Out
1	GND	Ground	N/A	26	N/C	No connect	N/A
2	IDESDR3	Data bit 3	I/O	27	IDESDR11	Data bit 11	I/O
3	IDESDR4	Data bit 4	I/O	28	IDESDR12	Data bit 12	I/O
4	IDESDR5	Data bit 5	I/O	29	IDESDR13	Data bit 13	I/O
5	IDESDR6	Data bit 6	I/O	30	IDESDR14	Data bit 14	I/O
6	IDESDR7	Data bit 7	I/O	31	IDESDR15	Data bit 15	I/O
7	IDESCS0X	IDE Chip Select 0	Out	32	IDESCS1X	IDE Chip Select 1	Out
8	GND	Ground	N/A	33	N/C	No connect	N/A
9	GND	Ground	N/A	34	IDESIORX	Read strobe	Out
10	GND	Ground	N/A	35	IDESIOWX	Write strobe	Out
11	GND	Ground	N/A	36	MSYS FD	M Systems FD Enable	In
12	GND	Ground	N/A	37	IDESINTR	Drive Interrupt Request	Out
13	VCC	Power	N/A	38	VCC	Power	N/A
14	GND	Ground	N/A	39	CF MAST	CompactFlash Master	In
15	GND	Ground	N/A	40	N/C	No connect	N/A
16	GND	Ground	N/A	41	IDESRSTX	Hard Drive reset	In
17	GND	Ground	N/A	42	IOCHRDY	IO Channel Ready	In
18	IDESA2	IDE Address 2	Out	43	N/C	No connect	N/A
19	IDESA1	IDE Address 1	Out	44	N/C	No connect	N/A
20	IDESA0	IDE Address 1	Out	45	HDDLED1	LED	Out
21	IDESDR0	Data bit 0	I/O	46	N/C	No connect	N/A
22	IDESDR1	Data bit 1	I/O	47	IDESDR8	Data bit 8	I/O
23	IDESDR2	Data bit 2	I/O	48	IDESDR9	Data bit 9	I/O
24	IDESIOCS16X	I/O Chip Select 16	In	49	IDESDR10	Data bit 10	I/O
25	N/C	No connect	N/A	50	GND	Ground	N/A

Table 18 Compact Flash Connector, J3

SVGA CRT/Flat-Panel Video Controller

The SystemCard 5MX provides a CRT/Flat-Panel video controller. It is hardware-level register compatible with existing PC video standards. It supports CRT-only, flat panel-only, and simultaneous display modes.

The controller uses 2M byes of system memory, which supports standard VGA resolutions and SVGA resolutions up to 1280 x 1024 in 256 colors.

CRT INTERFACE

The CRT video signals are brought out to J17, a 15-pin high density D-sub standard CRT connector. Pinouts for J17 are shown in Table 19. The system display options are: CRT only, 640 x 480 TFT, 800 x 600 TFT,

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1024 x 768 TFT and 1280 x 1024 TFT. Use the Custom Configuration screen to select the correct option (see page 37.

Pin	Signal	Function
1	IOUTR	Red
2	IOUTG	Green
3	IOUTB	Blue
9	VCCDDC	+5 Volts
12	DDCSDA	DDC Serial Data
13	HSYNCB	Horizontal Sync
14	VSYNCB	Vertical Sync
15	DDCSCL	DDC Serial Clock
5, 6 7, 8, 10	GND	Ground
4, 11	NC	No Connect

Table 19. CRT Connector, J17

FLAT-PANEL INTERFACE

Signals for various flat-panel displays, both color and gray scale, appear on connectors J15 and J33. The flat panel connector, J15, can be used to connect directly to a 12" Hitachi TFT or a 15" LG TFT flat panel. Table 20 lists the signals on J15.

J33 is designed to interface to a "daughter card," which in turn interfaces to a particular panel or family of panels. A daughter card provides for any additional circuitry that may be needed, such as contrast control logic, backlight power connections, Vee power supply converters, power sequencing and management circuits, and for the panel's specialized ribbon-cable connectors.

Table 21 lists the signals on J33. A full set of flat-panel signals is provided. Note that current flat panels do not share a standardized connector pin configuration. Even the names of panel control signals vary from manufacturer to manufacturer. Review the manufacturer's documentation to ascertain what signals are required to drive the flat panel you choose.

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Pin	Signal Name	Description	Pin	Signal Name	Description
1	GND	Ground	2	SHFCLK	Shift clock
3	GND	Ground	4	FPHSYNC	Horizontal sync
5	FPVSYNC	Vertical sync	6	GND	Ground
7	GND	Ground	8	GND	Ground
9	FPD12	Data 12	10	FPD13	Data 13
11	FPD14	Data 14	12	GND	Ground
13	FPD15	Data 15	14	FPD16	Data 16
15	FPD17	Data 17	16	GND	Ground
17	GND	Ground	18	GND	Ground
19	FPD6	Data 6	20	FPD7	Data 7
21	FPD8	Data 8	22	GND	Ground
23	FPD9	Data 9	24	FPD10	Data 10
25	FPD11	Data 11	26	GND	Ground
27	GND	Ground	28	GND	Ground
29	FPD0	Data 0	30	FPD1	Data 1
31	FPD2	Data 2	32	GND	Ground
33	FPD3	Data 3	34	FPD4	Data 4
35	FPD5	Data 5	36	GND	Ground
37	FPDISPEN	Display enable	38	NC	No connect
39	+3.3VDISP	3.3 Volts	40	+3.3VDISP	3.3 Volts
41	+3.3VDISP	3.3 Volts			

Table 20. Flat-Panel Interface Connector, J15

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Pin	Signal Name	Description	Pin	Signal Name	Description
1	GND	Ground	2	GND	Ground
3	FPVDDEN	VDD Enable	4	RESETX	Reset
5	FP VDDEN	VDD Enable	6	FPDISPENR	Display Enable
7	FPDR0	Data 0	8	FPDR1	Data 1
9	FPDR2	Data 2	10	FPDR3	Data 3
11	FPDR4	Data 4	12	FPDR5	Data 5
13	FPDR6	Data 6	14	FPVSYNCR	Vertical Sync
15	+3.3VDISP	3.3 Volts	16	+3.3VDISP	3.3 Volts
17	FPHSYNCR	Horizontal Sync	18	GND	Ground
19	GND	Ground	20	FPDR7	Data 7
21	FPDR8	Data 8	22	FPDR9	Data 9
23	FPDR10	Data 10	24	FPDR11	Data 11
25	FPDR12	Data 12	26	FPDR13	Data 13
27	FPDR14	Data 14	28	FPDR15	Data 15
29	FPDR16	Data 16	30	FPDR17	Data 17
31	DS_SCLK	Dual Scan Serial Clock	32	DS SDIN	Dual Scan Data In
33	GND	Ground	34	CLKFPCON	Flat Panel Clock
35	GND	Ground	36	DS_SCS	Dual Scan Chip Select
37	DS SDO	Dual Scan Data Out	38	DSDAC_CS	Contrast Chip Select
39	+5V	+5 Volts	40	BL BRIGHT	Brightness Control
41	NC	No connect	42	NC	No connect
43	GND	Ground	44	GND	Ground

Table 21. Flat-Panel Interface Connector, J33

FLAT-PANEL DISPLAY VOLTAGE

Current flat panels use either +5 volts or 3.3 volts. The SystemCard 5MX has an on-board voltage regulator to provide 3.3 volt control signals to a flat panel.

The flat panel backlight power connector, J16, is a 5 pin single row connector. The pinout for this connector is listed in Table 22.

Pin	Signal Name
1	No Connect
2	Brightness
3	+12 Volts
4	Ground
5	+12 Volts

Table 22. Flat Panel Backlight Power Connector, J16

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POWER SEQUENCING

Some LCD flat-panel displays require power sequencing to prevent damage. For example, some panels can be damaged if the Vee bias supply is applied to the panel without first powering the control and data lines. The flat-panel video controller provides control signals for sequencing the power in the proper order to protect the panel from these effects. (The video BIOS controls the sequence and timing of these signals.) The SystemCard 5MX supports automatic sequencing of Vdd (+5V), Vee (bias voltages typically in the range of -30V<Vee<+30V), and +12V (for an external backlight power inverter). Use the ENAVDD and ENAVEE signals to switch the Vdd and Vee voltages respectively.

Touchscreen Interface

The touchscreen interface is only available on the ZF netDisplay version of the SystemCard 5MX. It is based on the Elo E271-Coach Touchscreen controller. The touchscreen controller is designed for use with the Elo Touchsystems 5-wire resistive technology touchscreens.

The controller has a RS232 serial interface and uses COM2 on the SystemCard. The connector for the touchscreen is J28. The pinout for J28 is shown in Table 23.

Pin	Signal Name
1	L
2	Y
3	Sense
4	X
5	H

Table 23. Touchscreen connector, J28

Ethernet Controller

This section describes how to configure and connect the Ethernet LAN interface.

The setup utility for the Ethernet controller is RSET8139.EXE.

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector. This device is resident on the PCI bus.

In addition, software configuration of the Ethernet interface requires that you install compatible networking software:

- Install the proper driver for the network operating system you will be running.
- Use the network operating system (NOS) client install procedure provided by your NOS software vendor and follow their instructions.

CONNECTING TO THE ETHERNET CABLE

The Ethernet interface supports 100BaseT (twisted pair). The interface connector appears on connector J26. J26 is a RJ45 modular connector. The following table lists the signals and pin numbers of J26:

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Pin	Signal Name
1	+ Transmit Data
2	- Transmit Data
3	+ Receive Data
4	N/C
5	N/C
6	- Receive Data
7	N/C
8	N/C

Table 24. RJ45 Connector, J15

Audio Support

The audio circuitry is SoundBlaster compatible. The following table shows the resources used in the audio circuitry

Resource	Function
I/O Address 220h	SB compatible wave port
I/O Address 330h	Yamaha OPL2 midi
IRQ5	Wave engine IRQ
DMA 0	Wave engine 8-bit DMA
DMA 5	Wave engine 16-bit DMA

Table 25 Audio Resources

SPEAKER

Small piezoelectric speakers or standard PC speakers (with an 8 ohm coil) can be directly driven by the SystemCard 5MX through connector J14. The port supplies approximately 0.1 watt to the speaker. The speaker signal is TTL, current-limited with a series 33 ohm resistor. High frequencies are rolled off with a 0.01 µF capacitor (to ground).

Table 26 shows the pinout of J14.

Signal Name	Pin	Description
5V	1	+5 Volts
Spkrdrv	2	Signal
GND	3	Ground
Speaker -	4	Signal

Table 26. Speaker Connector, J14

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HEADPHONE OUT/MIC IN

The SystemCard 5MX has two stereo phone jacks. One is for a headphone at connector J12 and the other is for a microphone at connector J35.

CD/LINE IN

J10 is a four pin header to connect an audio input. Table 27 describes the pinout.

Signal Name	Pin	Description
LININR/CDINR	1	Right Audio Input
GND	2	Ground
GND	3	Ground
LININL/CDINL	4	Left Audio Input

Table 27 CD/Line In Connector, J10

USB Interface

The SystemCard 5MX has two independent Universal Serial Bus (USB) interfaces. Each port has a Data "–" and a Data "+"pin. The USB ports are Open Host Controller Interface (OpenHCI) compliant. The OpenHCI specification provides a register-level description for a host controller, as well as a common industry hardware/software interface and drivers.

The USB connector is a dual stacked, right angle connector. The pinout for J6 is shown in Table 28.

Signal Name	Pin	Description
USBVCC1	1	Port 1 Vcc
USBD1F+	2	Port 1 Data +
USBD1F-	3	Port 1 Data -
USBGND1	4	Port 1 Ground
USBVCC2	5	Port 2 Vcc
USBD2F+	6	Port 2 Data +
USBD2F-	7	Port 2 Data -
USBGND2	8	Port 2 Ground

Table 28. USB Connector, J6

Memory Expansion Socket

The board has one 32-pin byte-wide memory chip socket that can be used for additional storage. You can install any of a variety of 28-pin or 32-pin JEDEC-compliant memory devices, Flash, EPROM, NOVRAM (non-volatile static RAM with an internal backup battery), and Disk-On-Chip. If you use a Disk-On-Chip device, the sockets can emulate an additional disk drive. The Disk-On-Chip has a default address of D800h and a window of 32K.

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Note: If you install a 28-pin device in a socket, install pin 1 of the device in pin 3 of the socket. Leave pins 1, 2, 31, and 32 empty.

CONFIGURING THE MEMORY EXPANSION SOCKET

Configure the memory expansion socket using the Custom Setup Screen in the CMOS Setup. . The Custom Setup Screen allows you to configure the device, size and memory starting address.

Watchdog Timer

A watchdog timer is a circuit designed to reset your program or hardware, which is not running properly. It usually is implemented for processes or activities that have some time predictability, such as the length of time it takes to perform a particular software function or complete the movement (or other change) of some physical system.

A typical application, for example, would initialize the watchdog timer when certain software functions start and end, or when a limit switch or optical interrupter connected to one of the digital I/O pins changes state. If the software crashes or gets stuck in a loop, or if the mechanical switch is not closed, the watchdog timer times out, causing a system reset.

The SystemCard has a built-in configurable down counter that can be loaded with values from 00 to FFh (these correspond to delays of 0 to 255 seconds) to generate a timeout unless reset by its input signal, WDI. WDI is an internally-generated logic signal controlled by a BIOS call. As long as the timer is reset by the preset delay, its output signal, WDO remains in its inactive state. Should the timer time out, the WDO signal goes high, triggering a reset.

PC/104 Expansion Bus Interface

Table 29 documents the PC/104 expansion bus provided on the SystemCard. It also includes the pin designations for the standard ISA expansion bus interface signals for reference to standard PC bus expansion cards.

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PC/104 Pin	ISA	Signal Name	Function	In/out
A1	A1	IOCHCK-	Bus NMI input	In
A2	A2	SD7	System Data bit 7	I/O
A3	A3	SD6	System Data bit 6	I/O
A4	A4	SD5	System Data bit 5	I/O
A5	A5	SD4	System Data bit 4	I/O
A6	A6	SD3	System Data bit 3	I/O
A7	A7	SD2	System Data bit 2	I/O
A8	A8	SD1	System Data bit 1	I/O
A9	A9	SD0	System Data bit 0	I/O
A10	A10	IOCHRDY	Processor Ready Ctrl	In
A11	A11	AEN	Address Enable	I/O
A12	A12	SA19	Address bit 19	I/O
A13	A13	SA18	Address bit 18	I/O
A14	A14	SA17	Address bit 17	I/O
A15	A15	SA16	Address bit 16	I/O
A16	A16	SA15	Address bit 15	I/O
A17	A17	SA14	Address bit 14	I/O
A18	A18	SA13	Address bit 13	I/O
A19	A19	SA12	Address bit 12	I/O
A20	A20	SA11	Address bit 11	I/O
A21	A21	SA10	Address bit 10	I/O
A22	A22	SA9	Address bit 9	I/O
A23	A23	SA8	Address bit 8	I/O
A24	A24	SA7	Address bit 7	I/O
A25	A25	SA6	Address bit 6	I/O
A26	A26	SA5	Address bit 5	I/O
A27	A27	SA4	Address bit 4	I/O
A28	A28	SA3	Address bit 3	I/O
A29	A29	SA2	Address bit 2	I/O
A30	A30	SA1	Address bit 1	I/O
A31	A31	SA0	Address bit 0	I/O
A32		GND	Ground	N/A

Table 29. PC/104 Expansion Bus Connector, A1 – A32

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PC/104 Pin	ISA	Signal Name	Function	In/out
B1	B1	GND	Ground	N/A
B2	B2	RESETDRV	System reset signal	Out
B3	B3	+5V	+5 volts	N/A
B4	B4	IRQ9	Interrupt request 9	In
B5	B5	-5V	-5 volts	N/A
B6	B6	DRQ2	DMA request 2	In
B7	B7	-12V	-12 volts	N/A
B8	B8	ENDXFR- (0WS-)	End Transfer (Zero wait state)	In
B9	B9	+12V	+12 volts	N/A
B10	B10			
B11	B11	SMEMW-	Mem Write (lower 1MB)	I/O
B12	B12	SMEMR-	Mem Read (lower 1MB)	I/O
B13	B13	IOW-	I/O Write	I/O
B14	B14	IOR-	I/O Read	I/O
B15	B15	DACK3-	DMA Acknowledge 3	Out
B16	B16	DRQ3	DMA Request 3	In
B17	B17	DACK1-	DMA Acknowledge 1	Out
B18	B18	DRQ1	DMA Request 1	In
B19	B19	REFRESH-	Memory Refresh	I/O
B20	B20	SYSCLK	System clock (8 MHz)	Out
B21	B21	IRQ7	Interrupt Request 7	In
B22	B22	IRQ6	Interrupt Request 6	In
B23	B23	IRQ5	Interrupt Request 5	In
B24	B24	IRQ4	Interrupt Request 4	In
B25	B25	IRQ3	Interrupt Request 3	In
B26	B26	DACK2-	DMA Acknowledge 2	Out
B27	B27	TC	DMA Terminal Count	Out
B28	B28	BALE	Address latch enable	Out
B29	B29	+5V	+5 volt	N/A
B30	B30	OSC	14.318 MHz clock	Out
B31	B31	GND	Ground	N/A
B32		GND	Ground	N/A

Table 29. PC/104 Expansion Bus Connector, B1 – B32 (cont'd)

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PC/104 Pin	ISA	Signal name	Function	In/out
C0		GND	Ground	N/A
C1	C1	SBHE-	Bus High Enable	I/O
C2	C2	LA23	Address bit 23	I/O
C3	C3	LA22	Address bit 22	I/O
C4	C4	LA21	Address bit 21	I/O
C5	C5	LA20	Address bit 20	I/O
C6	C6	LA19	Address bit 19	I/O
C7	C7	LA18	Address bit 18	I/O
C8	C8	LA17	Address bit 17	I/O
C9	C9	MEMR-	Memory Read	I/O
C10	C10	MEMW-	Memory Write	I/O
C11	C11	SD8	System Data bit 8	I/O
C12	C12	SD9	System Data bit 9	I/O
C13	C13	SD10	System Data bit 10	I/O
C14	C14	SD11	System Data bit 11	I/O
C15	C15	SD12	System Data bit 12	I/O
C16	C16	SD13	System Data bit 13	I/O
C17	C17	SD14	System Data bit 14	I/O
C18	C18	SD15	System Data bit 15	I/O
C19		GND	Ground	N/A

Table 29. PC/104 Expansion Bus Connector, C0 – C19 (cont'd)

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PC/104 Pin	ISA	Signal Name	Function	In/out
D0		GND	Ground	N/A
D1	D1	MEMCS16-	16-bit memory access	In
D2	D2	IOCS16-	16-bit I/O access	In
D3	D3	IRQ10	Interrupt Request 10	In
D4	D4	IRQ11	Interrupt Request 11	In
D5	D5	IRQ12	Interrupt Request 12	In
D6	D6	IRQ15	Interrupt Request 15	In
D7	D7	IRQ14	Interrupt Request 14	In
D8	D8	DACK0-	DMA Acknowledge 0	Out
D9	D9	DRQ0	DMA Request 0	In
D10	D10	DACK5-	DMA Acknowledge 5	Out
D11	D11	DRQ5	DMA Request 5	In
D12	D12	DACK6-	DMA Acknowledge 6	Out
D13	D13	DRQ6	DMA Request 6	In
D14	D14	DACK7-	DMA Acknowledge 7	Out
D15	D15	DRQ7	DMA Request 7	In
D16	D16	+5V	+5 volt	N/A
D17	D17	MASTER-	Bus master assert	In
D18	D18	GND	Ground	N/A
D19		GND	Ground	N/A

Table 29. PC/104 Expansion Bus Connector, D0 – D19 (cont'd)

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PCI Expansion Bus

Table 30 documents the PCI expansion bus provided on the SystemCard 5MX at J21.

PCI Bus Pin	Signal Name	Function
A1	PTRSTX	Test Reset
A2	12V	+12 Volts
A3	PTMS	Test Mode Select
A4	PTDI	Test Input
A5	5V	+5 Volts
A6	INTBX	PCI Interrupt B
A7	INTDX	PCI Interrupt D
A8	5V	+5 Volts
A9	N/C	No Connect
A10	5V	+5 Volts
A11	N/C	No Connect
A12	GND	Ground
A13	GND	Ground
A14	N/C	No Connect
A15	PRSTX	PCI Reset
A16	5V	+5 Volts
A17	PGNT1X	Grant Line 1
A18	GND	Ground
A19	PMEX	Power Management Enable
A20	PAD30	Address/Data 30
A21	3V	+3 Volts
A22	PAD28	Address/Data 28
A23	PAD26	Address/Data 26
A24	GND	Ground
A25	PAD24	Address/Data 24
A26	PIDSEL1	Initialization Device Select 1
A27	3V	+3 Volts
A28	PAD22	Address/Data 22
A29	PAD20	Address/Data 20
A30	GND	Ground
A31	PAD18	Address/Data 18

Table 30. PCI Bus Connector, J21

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PCI Bus Pin	Signal Name	Function
A32	PAD16	Address/Data 16
A33	3V	+3 Volts
A34	FRAMEX	Cycle Frame
A35	GND	Ground
A36	TRDYX	Target Ready
A37	GND	Ground
A38	STOPX	Target Stop
A39	3V	+3 Volts
A40	SDONE	Snoop Done
A41	SBOX	Snoop Back Off
A42	GND	Ground
A43	PPAR	Parity
A44	PAD15	Address/Data 15
A45	3V	+3 Volts
A46	PAD13	Address/Data 13
A47	PAD11	Address/Data 11
A48	GND	Ground
A49	PAD9	Address/Data 9
A52	PCBE0X	Command & Byte Enable 0
A53	3V	+3 Volts
A54	PAD6	Address/Data 6
A55	PAD4	Address/Data 4
A56	GND	Ground
A57	PAD2	Address/Data 2
A58	PAD0	Address/Data 0
A59	5V	+5 Volts
A60	PREQ64AX	Request 64-bit Transfer
A61	5V	+5 Volts
A62	5V	+5 Volts

Table 30 - PCI Expansion Bus Connector, J21 (cont'd)

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PCI Bus Pin	Signal Name	Function
B1	-12V	-12 Volts
B2	PTCK	Test Clock
B3	GND	Ground
B4	N/C	No Connect
B5	5V	+5 Volts
B6	5V	+5 Volts
B7	INTCX	PCI Interrupt C
B8	INTAX	PCI Interrupt A
B9	PRSNT1AX	Card Present 1A
B10	N/C	No Connect
B11	PRSNT1BX	Card Present 1B
B12	GND	Ground
B13	GND	Ground
B14	N/C	No Connect
B15	GND	Ground
B16	CLKPCISL1	Clock Select 1
B17	GND	Ground
B18	PREQ1X	Request Line 1
B19	5V	+5 Volts
B20	PAD31	Address/Data 31
B21	PAD29	Address/Data 29
B22	GND	Ground
B23	PAD27	Address/Data 27
B24	PAD25	Address/Data 25
B25	3V	+3 Volts
B26	PCBE3X	Command & Byte Enable 3
B27	PAD23	Address/Data 23
B28	GND	Ground
B29	PAD21	Address/Data 21
B30	PAD19	Address/Data 19

Table 30. PCI Bus Connector, J21 (cont'd)

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PCI Bus Pin	Signal Name	Function
B31	3V	+3 Volts
B32	PAD17	Address/Data 17
B33	PCBE2X	Command & Enable 2
B34	GND	Ground
B35	IRDYX	Initiator Ready
B36	3V	+3 Volts
B37	DEVSELX	Device Select
B38	GND	Ground
B39	LOCKX	Lock Operation
B40	PERRX	Parity Error
B41	GND	Ground
B42	SERRX	System Error
B43	3V	+3 Volts
B44	PCBE1X	Command & Byte Enable
B45	PAD14	Address/Data 14
B46	GND	Ground
B47	PAD12	Address/Data 12
B48	PAD10	Address/Data 10
B49	GND	Ground
B52	PAD8	Address/Data 8
B53	PAD7	Address/Data 7
B54	3V	+3 Volts
B55	PAD5	Address/Data 5
B56	PAD3	Address/Data 3
B57	GND	Ground
B58	PAD1	Address/Data 1
B59	5V	+5 Volts
B60	PACK64X	Acknowledge 64-bit Transfer
B61	5V	+5 Volts
B62	5V	+5 Volts

Table 30 - PCI Expansion Bus Connector, J21 (cont'd)

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BIOS Setup

The SystemCard 5MX system BIOS (Basic Input Output System) supports a standard Setup function to configure system parameters (as well as advanced methods specifically designed for embedded systems). The BIOS uses the Setup parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Setup parameters are normally stored in the CMOS configuration memory, a portion of the real-time-clock circuit.

USING SETUP

To enter the Setup function, press the <Del> key during POST. <Del> can be asserted at any time prior to boot.

Note: When you change Setup parameters, the new values do not take effect until the system is rebooted.

There are seven options in the Setup function:

- **Basic CMOS Configuration** — Displays the standard CMOS options you can set for your system.
- **Custom Configuration** — Displays the custom CMOS options you can set for your system.
- **Format Integrated Flash Disk** — This is a low level format. You must still use a DOS format command.
- **Reset CMOS to last known values**
- **Reset CMOS to factory defaults** — The factory defaults are as follows:
 - ⇒ Drive A: = Floppy 0 (1.44MB) 2nd Boot Device
 - ⇒ Drive B: = none
 - ⇒ Drive C: = IDE 0, PM (Type 3) 1st Boot Device
 - ⇒ Drive D: = IDE 2, SM (Type 2)
 - ⇒ System display = 800 x 600 TFT
 - ⇒ Console Redirection = Probe COM1
 - ⇒ Redirection Speed = 19.2K
- **Write to CMOS and Exit** —this option allows you to save new CMOS values.
- **Exit without changing CMOS** —this option allows you to exit from setup without modifying the CMOS.

Basic CMOS Configuration Options

The following options can be set on the Basic CMOS Configuration screen.

- **Drive A:** and **Drive B:**—Select which drive you have connected for the A: and B: drives. Choices available include: Floppy 0, Floppy 1, Flash disk, and NONE.
- **Drive C:** and **Drive D:**—Select which drive you have connected for the C: and D: drives. Choices are Floppy 0, Floppy 1, Flash disk, IDE 0 PM(Primary Master), IDE 1 PS(Primary Slave), IDE 2 SM(Secondary Master), IDE 3 SS(Secondary Slave), and NONE

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- **Drive E:** through **Drive K:** — Select which hard drive you have connected for the E:, F:, G:, H:, I:, J:,K:. Choices are IDE 0 PM(Primary Master), IDE 1 PS(Primary Slave), IDE 2 SM(Secondary Master), IDE 3 SS(Secondary Slave), and NONE
- **Floppy 0** and **Floppy 1**—Select which type of floppy drive you have connected. Choose from the following options: 360K, 1.2M, 720K, 1.44M, 2.88M, and NOT INSTALLED.
- **IDE 0** through **IDE 3**—Select the drive type of the hard disk you have installed in your system.
 - IDE0 is designated Primary Master (PM); IDE1 is designated Primary Slave (PS); IDE2 is designated Secondary Master (SM); and IDE3 is designated Secondary Slave (SS).
 - Use drive type 1 if you want to enter specific values for your drive. To find out what values to enter, use the drive manufacturer's documentation.
 - Use drive type 2 for Autodetect. Most newer drives will respond with their drive values when queried by the BIOS. A SanDisk is also set up as a type 2.
 - Use drive type 3 for LBA geometry.
 - Use drive type 4 for phoenix CHS geometry.
 - Use Not Installed for a solid state disk, such as DiskOnChip or no disk.
- **1st Boot Device, 2nd Boot Device, 3rd Boot Device, and 4th Boot Device**—These fields are used to select the order the system follows when attempting to boot. For example, the system first tries to boot from the "1st Boot Device" and if it can't then tries the "2nd Boot Device" and so on, until a boot drive is found. The following choices are supported:

– >Drive A:, >Drive B:, >Drive C:,… Drive K Boot from the drive identifier entered

– >Debugger

– >WinCE

– DOS-ROM

– Mfg. Mode

Note: Debugger, WinCE, DOS-ROM, and Mfg. Mode are not supported in the BIOS.

Custom Configuration screen

The options in the Custom Configuration screen are as follows:

- **System Display**—You can choose between the following options: CRT only; 640 x 480 TFT flat panel; 800 x 600 TFT flat panel; and 1024 x 768 TFT flat panel
- **Infrared at COM1**—This option is not available at this time.
- **Console Redirection** —The options are Disabled; Probe COM1; Probe COM2; Probe COM3; Probe COM4; Always COM1; Always COM2; Always COM3; Always COM4
- **Redirection Speed** —You have a choice of several different baud rates, but 19.2K is recommended.

Backup Fail Safe ROM

In addition to the system's BIOS, the SystemCard 5MX has a *Safe Mode* ROM (in a separate ROM), known as BDIS, that you can use to boot your system. You would use this feature if the BIOS fails, if the CMOS RAM is configured to put the SystemCard in a non-recoverable state, or when recovering from an interrupted or failed upgrade attempt of the SystemCard's BIOS.

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The *Safe Mode* ROM has the same functions as the main BIOS. It can boot from a floppy disk, output to video, take keyboard inputs, and so forth. It uses the same CMOS setup information as the BIOS.

To boot your system using the Safe Mode ROM, install a jumper on the two pin header at J34. This enables the boot ROM and disables the BIOS. Apply power to your system. You should have a keyboard and monitor attached.

Specifications

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Voltage on any pin, with respect to Ground -0.3V to +6.5V

Storage Temperature (case)-55°C to +80°C (-67°F to +176°F)

OPERATING CONDITIONS*

Supply Voltage (V_{CC}) 4.75V to +5.25V

Case Temperature (under bias) 0°C to 70°C (32°F to 158°F)

* Stresses above those listed above can cause permanent damage to the board. These values are stress ratings only and do not imply that the device should be operated at these extremes. Exposure beyond the "Operating Conditions" may affect device reliability. Note that some power supplies exhibit voltage spikes when AC power is switched on or off or when voltage transients appear on the AC power line. If this possibility exists it is suggested that you use a clamp circuit on the DC supply.

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Literature References

The following references are for information about the PC architecture, the microprocessor, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
CompuServe: 72507,1054
Published by Addison Wesley, Inc.
http://www.mindshare.com

AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6
http://www.annabooks.com

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854
http://www.ieee.org

MS-DOS References

MS-DOS Functions, Ray Duncan, Microsoft Press
MS-DOS Programmer's Reference, Microsoft Press, Microsoft Corporation
Undocumented DOS, Andrew Schulmen, Addison/Wesley

Technical data on the 5MX microprocessor:

National Semiconductor
2900 Semiconductor Drive
Santa Clara, CA 95050
Phone: 1-800-272-9959
FAX: 1-800-737-7018
Email: support@nsc.com
http://www.national.com

Technical data on Embedded DOS 6-XL

General Software, Incorporated
P.O. Box 2571
Redmond, WA 98073
Phone: (206)454-5755
FAX: (206) 454-5744
Email: general@gensoft.wa.com
BBS: (206) 454-5894

The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0
Lotus Development Corporation
55 Cambridge Parkway
Cambridge, MA 02142

PC/104 Consortium

809 B-175 Cuesta Drive,
Mountain View, CA 94040
Phone: 415 903-8304
FAX: 415 967-0995

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MANUAL REVISIONS

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